

APR 07 2000  
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Application Number

09/498,739

Logically

Chiun-Chi Shen

Filing Date

02/07/00

Group Art Unit

2824

U. S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

[illegible]

## OTHER DOCUMENTS (Including Author, Title, Date, Portion or Pages, Etc.)

HN	<p>Saeki et al., "A 2.5-ns Clock Access, 250-MHz, 246-Mb SDRAM with Synchronous Mirror Delay," IEEE Journal of Solid State Circuits, Vol. 31, No. 11, Nov. 1996, pp. 1656-1664.</p>
HN	<p>Mamada et al., "Capacitance coupled Bus with Negative Delay Circuit for High speed and Low Power (10GB/s &lt; 500mW) Synchronous DRAMs," Digest of Papers for IEEE Symp. on VLSI Circuits, 1996, pp. 112-113.</p>
EXAMINER	<p>HIEN NGUYEN</p>
DATE CONSIDERED	<p>3/9/01</p>

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.